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Claims

[c1] 1.A method for fabricating a vertical bipolar junction transistor on a semiconductor wafer including a first doping region of a first conductivity type, a second doping region of a second conductivity type, and a plurality of isolated structures positioned on surfaces of the first doping region and the second doping region, the method comprising:
forming a third doping region of the first conductivity type in an upper portion of the second doping region;
forming a shielding layer on the surface of the semiconductor wafer;
removing a portion of the shielding layer to form an opening within the shielding layer to expose a portion of the third doping region;
forming a doping layer of the second conductivity type on a surface of the third doping region; and
performing a self-aligned silicidation process to form a silicide layer on the surfaces of the first doping region, the second doping region, the third doping region, and the doping layer, the silicide layer functioning as a contact region of the vertical bipolar junction transistor.

[c2] 2. The method of claim 1 wherein said isolated structures are formed by shallow trench isolation (STI).

[c3] 3. The method of claim 1 wherein said isolated structures are formed by local oxidation of silicon (LOCOS).

[c4] 4. The method of claim 1 wherein said second doping region more includes at least one heavy doping region of the second conductivity type.

[c5] 5. The method of claim 1 wherein said shielding layer includes oxide and/or silicon nitride.

[c6] 6. The method of claim 1 wherein said doping layer is made substantially from epitaxy/ amorphous silicon/ polysilicon.

[c7] 7. The method of claim 1 wherein said self-aligned silicidation process further includes forming an SAB layer on the surface of a portion of the doping layer, and forming at least one spacer on the surface of a side of the doping layer before said process.

[c8] 8. The method of claim 1 wherein said first conductivity type is P-type and said second conductivity type is N-type.

[c9] 9. The method of claim 1 wherein said first conductivity type is N-type and said second conductivity type is P-

type.

[c10] 10. The method of claim 1 wherein a surface of said semiconductor wafer further includes a CMOS, and a same implant process is performed to form said third doping region and at least one source /drain of the CMOS.

[c11] 11. The method of claim 1 wherein said doping layer further includes a heavy doping region of the second conductivity type to reduce the resistance of the doping layer.

[c12] 12.A method for fabricating a vertical bipolar junction transistor on a semiconductor wafer including a first doping region of N-type, a second doping region of P-type, and a plurality of isolated structures positioned on surfaces of the first doping region and the second doping region, the method comprising:
forming a third doping region of N-type in an upper portion of the second doping region;
forming a shielding layer on the surface of the semiconductor wafer; a portion of the shielding layer being removed to form an opening within the shielding layer to expose a portion of the third doping region;
forming a doping layer of P-type on a surface of the third doping region; and

performing a self-aligned silicidation process to form a silicide layer on the surfaces of the first doping region, the second doping region, the third doping region, and the doping layer , the silicide layer functioning as a contact region of the vertical bipolar junction transistor.

[c13] 13. The method of claim 12 wherein said isolated structures are formed by shallow trench isolation (STI).

[c14] 14. The method of claim 12 wherein said isolated structures are formed by local oxidation of silicon (LOCOS).

[c15] 15. The method of claim 12 wherein said second doping region more includes at least one heavy doping region of P-type.

[c16] 16. The method of claim 12, wherein said shielding layer includes oxide and/or silicon nitride.

[c17] 17. The method of claim 12 wherein said doping layer is made substantially from epitaxy/ amorphous silicon/ polysilicon.

[c18] 18. The method of claim 12 wherein said self-aligned silicidation process further includes forming an SAB layer on the surface of a portion of the doping layer, and forming at least one spacer on the surface of a side of the doping layer before said process.

[c19] 19. The method of claim 12 wherein a surface of said semiconductor wafer further includes a CMOS, and a same implant process is performed to form said third doping region and at least one source /drain of the CMOS.

[c20] 20. The method of claim 12 wherein said doping layer further includes a heavy doping region of P-type to reduce the resistance of the doping layer.